# Signal Processing For Power Amplifiers

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# Outline

- Motivation and Requirements
  - Cost impact
- Architecture and Algorithms
  - CFR
  - DPD & MEC
  - MEQ
- Simulation
  - Environment
  - Results
- Emerging Solutions and Future Directions
  - Design Directions
  - Conclusions

# Motivation

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# The Need For Linearization

- PA performance effects Carrier Expenses
- Digital Linearization techniques enable:
  - CapEx Reduction due to lower cost BTS (10-15%)
    - Remove gain stages, circuit hand tuning
  - OpEx reduction due to higher efficiency PA
    - Current designs lose ~85% of PA power as heat
    - Annual electrical costs avg ~$2500 per BTS
- Performance targets
  - Double efficiency of PA (from 12% to 25%)
  - Increase ACLR by > 30 dB
    - Better than -45 dBc ACLR
  - Improve OBO by more than 4 dB
  - Less than 17.5% EVM

# Architecture and Algorithms

- Motivation and Requirements
  - Cost impact
  - Higher density systems
- Architecture and Algorithms
  - Crest Factor Reduction CFR
  - Digital Pre-Distortion & Memory Effects Comp DPD & MEC
  - Modulator Equalization MEQ
- Simulation
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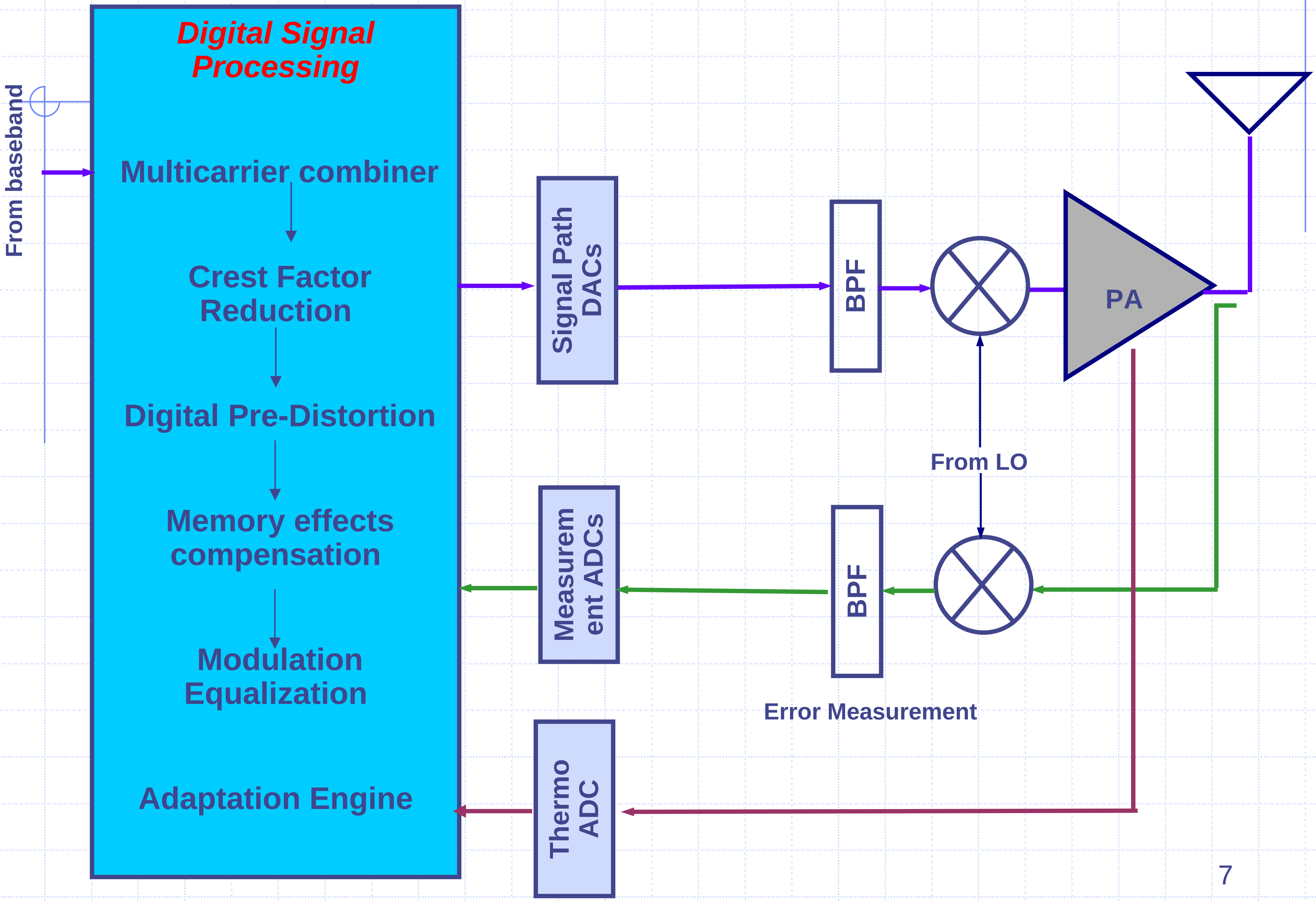
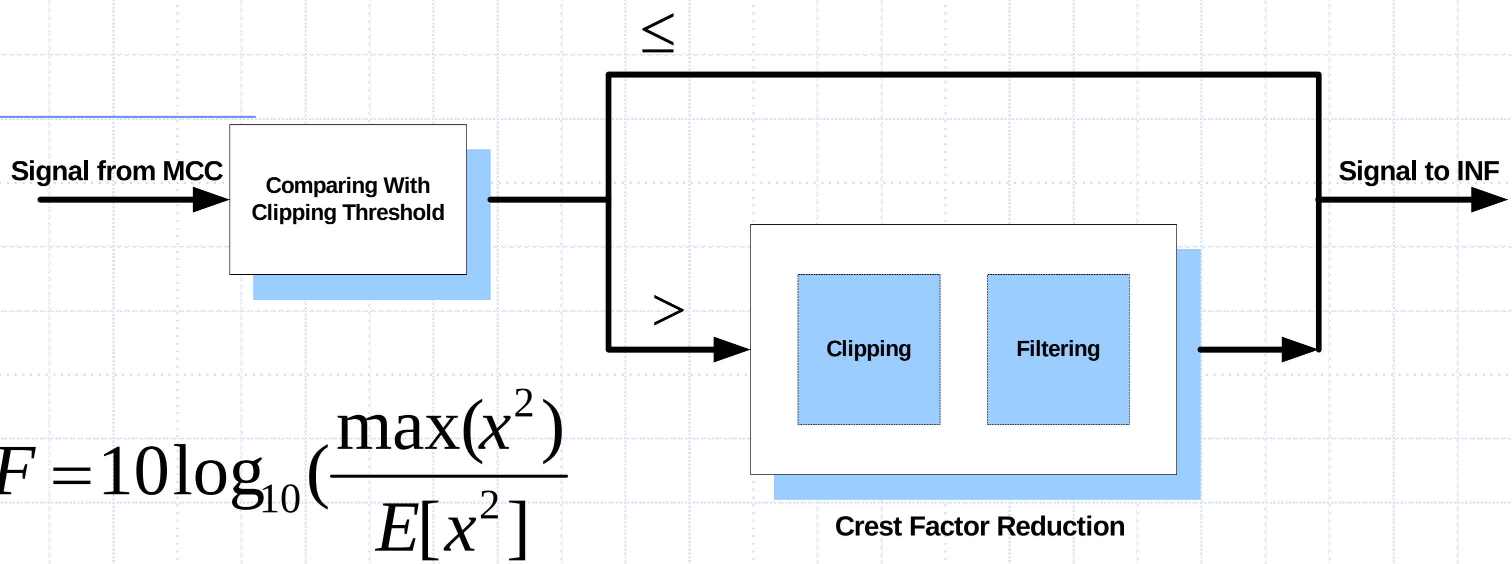
# Signal Processing Features

- Crest factor reduction (CFR)
  - Provides more than 6dB improvement in PAR by reducing peak excursions
  - Goodness by measuring EVM, PCDE and ACLR
- Digital pre-distortion (DPD)
  - Correction of gain non-linearity
  - Memory effects (temperature) correction
- Modulator Equalization (MEQ)
  - corrects impairments in analog modulator
    - Phase and gain imbalance, DC offsets

# Architecture Overview



# CFR Principles




$$CF = 10\log_{10}\left(\frac{\max(x^2)}{E[x^2]}\right)$$

$$PCDE = 10\log_{10}\left(\frac{\max(E[e_k^2])}{E[r'^2]}\right)$$

$$EVM_{RMS} = \sqrt{\frac{E[e^2]}{E[r^2]}}$$

- When magnitude exceeds threshold, CFR is performed.
- The basis of most CFR algorithms is clipping + filtering

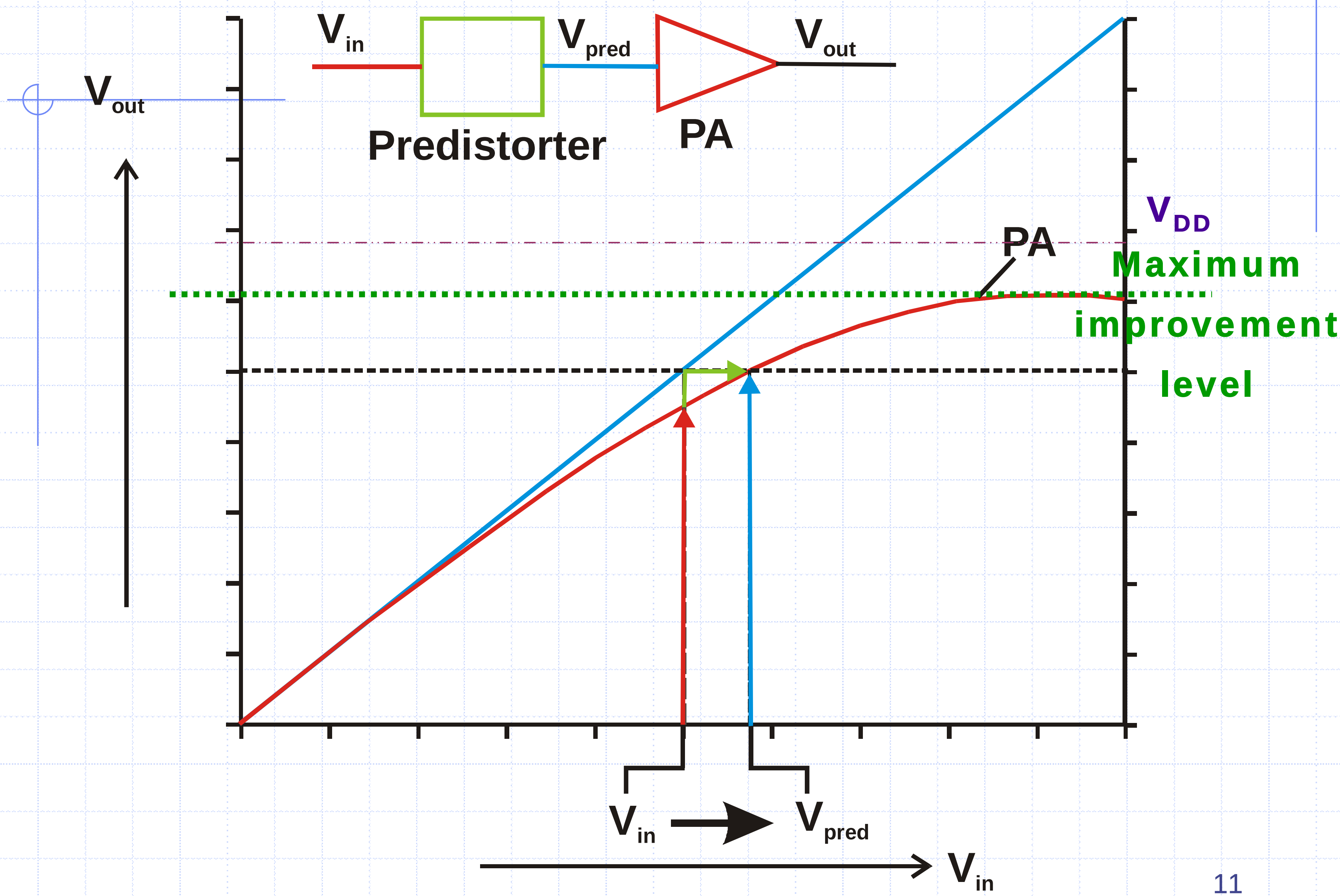
# Overview of CFR Algorithms

| Algorithm | ACLR | EVM | PCDE | COMMENTS |
|---|---|---|---|---|
| **Clipping** | High | Low | Medium | Simplest technique. |
| **Peak Windowing** | Medium | Medium | Medium | Window length a compromise between ACLR and EVM. |
| **Peak Cancellation** | Low | Medium | Medium | Similar to clipping and filtering. |
| **Dynamic Phase Distortion** | High | Low | Low | The phase distortion should be dynamically distributed among different carriers. |
| **Error Shaping** | Low | Low | Low | Peak regrowth is the main problem. |
| **Carrier Phase Alignment** | Low | Low | Low | Low complexity. |

# Memory Effects

- Slow memory effects
  - Supply voltage variation
  - Aging
  - Ambient temperature
  - Channel switching
- Fast memory Effects
  - Fast memory effects refer to those which occur so fast that we can not correct them with an adaptation (e.g. LMS) of a predistortion table

# Digital Predistortion



# Digital Predistortion

- Look Up Table for slow memory effects
- Polynomial for fast memory effects
- Training at startup followed by adaptation
- DPD LUT uses simple well known techniques
  - LMS: Well understood, converges for monotonic non-linearity's
  - RLS: For faster convergence
- Adaptation rate (~us) = impairments
- Adaptation engine operates on decimated signal

# Fast Memory Effects

- Fast memory effects create a floor where DPD becomes ineffective, hence we predict thermally induced distortion
  - Prediction provides correction faster then LUT
  - Prediction error measured in real time and improved in non-real time
- Initial correction based on initial calibration
- Modeled with a polynomial to predict gain compression
- Die temperature determined by signal envelope

# Modulator Equalization

- Simplifies analog/IF design
- Corrects for modulator and DAC imperfections
  - Gain and phase imbalance
  - DC offset
- Gradient descent for 6 parameters
- Initial calibration the adaptation during system operation

# Measurement Interface

- Measures AM/AM and AM/PM distortion
- Operates at $F_{composite}$
  - Uses generalized sampling theorem [Zhou]
  - Low cost ADC
- Hardware decimation and averaging of correction signal

# Simulation

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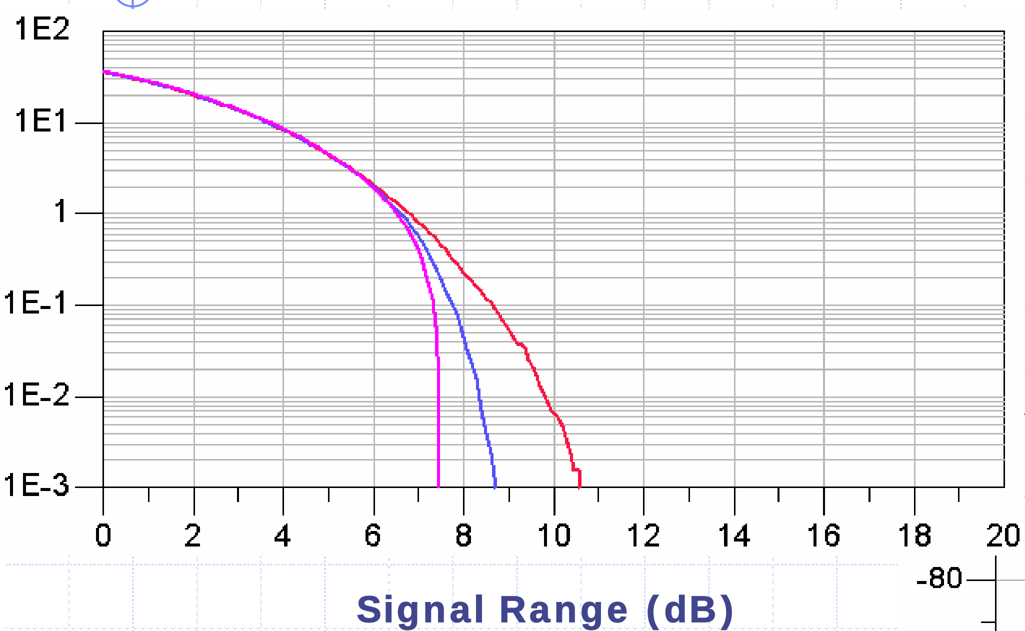
# Simulation Environment

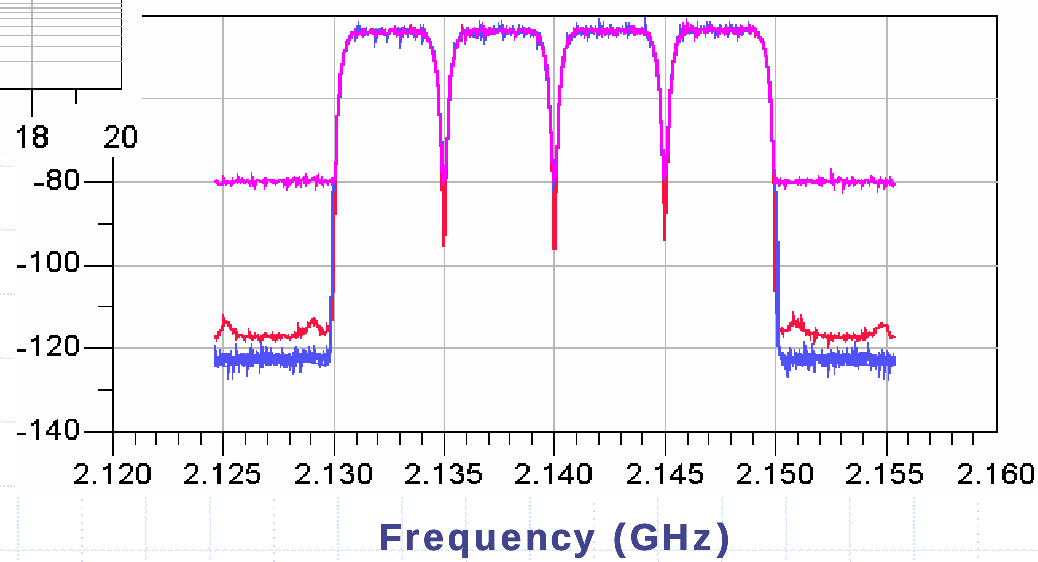
- 4 carrier WCDMA
- Agilent ADS simulation platform
  - Digital simulation in Ptolemy
  - Co-simulated sequential algorithms with MatLab
  - RF amplifier modeled with eesof (AET)
- Adaptive peak windowing (Matlab)
- Bit accurate models using ~14 – 16 bits
- Simple adaptation algorithm (MSE)

# CFR Results

**CCDF**

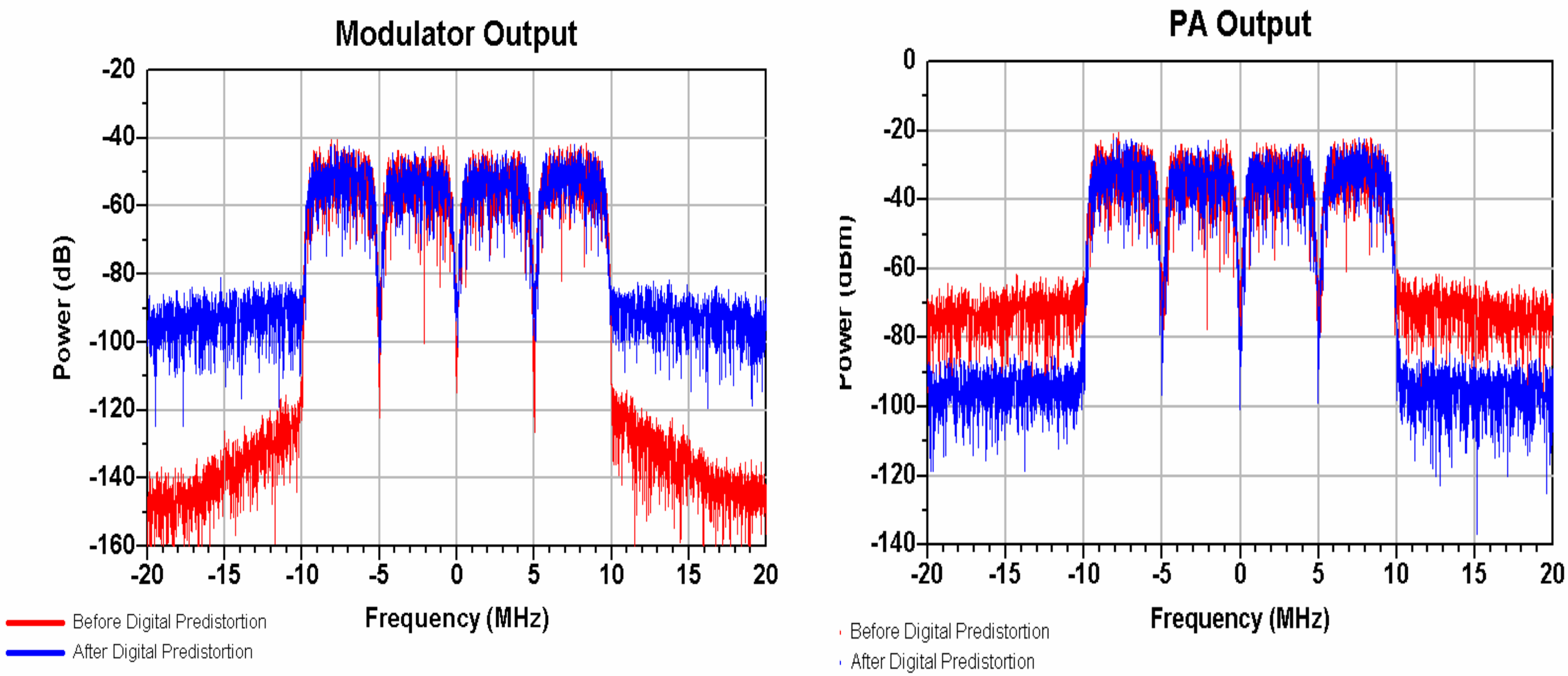



**Spectrum**




- Original WCDMA signal
- After clipping
- After clipping + filtering

# DPD Results


Modulator Output
Power (dB)
Frequency (MHz)
Before Digital Predistortion
After Digital Predistortion
PA Output
Power (dBm)
Frequency (MHz)
Before Digital Predistortion
After Digital Predistortion

# Emerging Solutions and Future Directions

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# Design Directions

- High levels of digital integration (following Moore's law) are possible thus allowing improvements in system performance with complex, but low cost and low power digital circuitry.
- Synergistic engineering at the module level enables these promise of higher linearity and efficiencies.

# Conclusion

- Total system design requires skills from packaging, RF design, Materials scientist and DSP designers
- High linearity and efficiency is achievable
- New applications can benefit from DPD technology
- “Old” architecture can have new lives

*Thank You!*